

CRYSTALLINE SILICON PV TECHNOLOGY ROADMAPMING IN THE CRYSTALCLEAR INTEGRATED PROJECT



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ABSTRACT: CrystalClear is an Integrated Project carried out in the 6th Framework Program of the European Union. The main project aim is to reduce the direct manufacturing costs of crystalline silicon PV modules to 1 €/Wp, when produced in next-generation plants. CrystalClear deals with the entire crystalline silicon value chain from silicon feedstock up to module manufacturing. Since many combinations of options for cell and module design, processing and materials may potentially fulfil the project aims, careful prioritization and selection of research topics is crucial. Moreover, research performed on the different parts of the chain has to be carefully coordinated and integrated in order to achieve results on a project level. In CrystalClear this process is performed through technology roadmapping, in combination with cost calculations and environmental analyses. This paper described the process and the results of roadmapping and cost calculations. Results of environmental analyses have been published elsewhere by E.A. Alsema et al. (see the CrystalClear project website). It is found that crystalline silicon PV technology indeed has the potential for direct module manufacturing costs of 1 €/Wp, or even less. This confirms the numbers in the recently published Strategic Research Agenda of the PV Technology Platform, see www.eupvplatform.org. Critical conditions to reach the target cost level are: efficient silicon utilization (g/Wp module power), high total area module efficiency and high-throughput, high-yield production.

Keywords: Cost reduction, PV Module, c-Si, Silicon, EU Project.

1 INTRODUCTION

CrystalClear (CC) is a large, 5-year joint effort of a powerful consortium of European companies, research institutes and university groups involved in crystalline silicon PV technology, see also www.ipcrystalclear.info. It is an Integrated Project carried out in the 6th Framework Program of the EU. The overall aims of CrystalClear are:

- research, development, and integration of innovative manufacturing technologies that allow solar modules to be produced at a cost of 1 €/Wp in next generation plants;
- improvement of the environmental profile of solar modules by the reduction of materials consumption, replacement of materials and designing for recycling;
- enhancement of the applicability of modules and strengthening of the competitive position of photovoltaics by tailoring to customer needs and improving product lifetime and reliability.

Realisation of these aims is a necessary condition for the European PV industry to maintain and strengthen its position on the world market and for photovoltaics to fulfil the expectations and policy targets.

CrystalClear runs from January 2004 to December 2008 and has a total budget of 28 M€. Of this amount 16 M€ will be contributed by the EU and 12 M€ by the 16 partners:

Industry partners:

- BP Solar (ES);
- Deutsche Cell (DE);
- Deutsche Solar (DE);
- Isofoton (ES);
- Photowatt (FR);
- REC (NO);
- Scanwafer (NO);
- Shell Solar; as of 1 July 2006 all activities have been transferred to SolarWorld (DE);
- Schott Solar (DE).

Universities:

- Konstanz (DE);
- UPM-IES (ES);
- Utrecht (NL).

Research institutes:

- CNRS InESS (FR)
- ECN (*coordinator*, NL);
- Fraunhofer-ISE (DE);
- IMEC (BE).

2 WHY TECHNOLOGY ROADMAPPING?

CrystalClear deals with the entire crystalline silicon value chain from silicon feedstock up to module manufacturing. Since many combinations of options for cell and module design, processing and materials may potentially fulfil the project aims, careful prioritization and selection of research topics is crucial. Moreover, research performed on the different parts of the chain has to be carefully coordinated and integrated in order to achieve results on a project level. In CrystalClear this process is performed through *technology roadmapping*, in combination with cost calculations and environmental analyses.

3 ROADMAPING APPROACH

The roadmapping approach chosen in CrystalClear starts with an inventory of the technology options space, i.e. a description of the choices that have to be made in order to construct so-called CrystalClear overall technologies, see Figure 1.

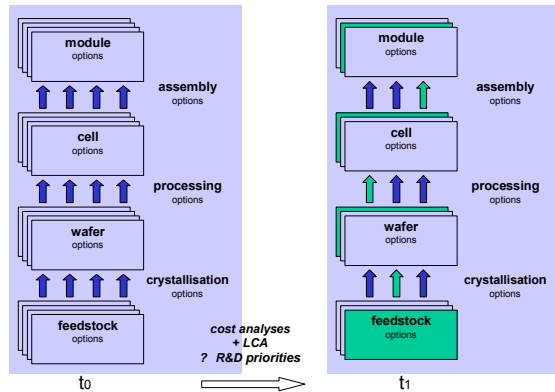


Figure 1: Technology options available to construct overall technologies.

The figure shows schematically how overall technologies may be built using different combinations of the available options for feedstock, crystallization & wafering, cell design & processing, and modules design & assembly. The overall technologies are then analysed according to the “drivers” for PV module development [1]. The main drivers considered here are:

1. manufacturing costs, including process yield effects, as a function of module efficiency;
2. environmental quality:
 - a. energy pay-back time;
 - b. (other) impact of materials and processes used;
3. versatility & flexibility (use anywhere and multipurpose).

It is noted that module manufacturing costs (€/Wp) should be considered in relation with module efficiency,

since a higher efficiency leads to lower (area related) system costs, allowing for higher module costs.

As it is not considered useful to start constructing overall technologies “from scratch”, we have started by choosing combinations of options that are known or expected to be effective in terms of cost, manufacturability or efficiency. The combinations were selected to cover a range of potentials for cost reduction and corresponding development risk profiles and development times, and crystalline silicon technology families (Cz single crystal silicon, cast multicrystalline silicon, ribbon silicon and thin-film silicon wafer equivalents).

As an example, Figure 2 shows the technology options for cell design. These options are interrelated to the module options in Figure 3.

1 Front junction (np or pn)	1.1 Front and rear electrodes (front and rear interconnects)	1.1.1 Rear surface not effectively passivated ^{*)} 1.1.2 Rear surface effectively passivated ^{*)}
	1.2 Metallization wrap through, MWT (rear interconnects)	1.2.1 Rear surface not effectively passivated 1.2.2 Rear surface effectively passivated
	1.3 Emitter wrap through, EWT (rear interconnects)	1.3.1 Rear surface not effectively passivated 1.3.2 Rear surface effectively passivated
2 Interdigitated rear junction (rear interconnects) with passivated front and rear surfaces		

^{*)} Passivation is a relative parameter as far as influence on cell performance is concerned; the degree of passivation roughly refers to the influence of silicon surface versus that of the silicon volume.

Figure 2: Cell design options considered.

1 Front-to-back interconnection (tabbing)	1.1 Soldering / welding / other HT methods	1.1.1 Glass front & foil lamination (= conventional) 1.1.2 Other encapsulation concepts (including one-material & roll lamination)
	1.2 Laser soldering	1.2.1 Glass front & foil lamination (= conventional) 1.2.2 Other encapsulation concepts (including one-material & roll lamination)
	1.3 Conductive adhesives	1.3.1 Glass front & foil lamination (= conventional) 1.3.2 Other encapsulation concepts (including one-material & roll lamination)
	1.4 Mechanical clamping (glass/low pressure/glass)	
2 Back-to-back interconnection	2.1 Soldering / welding / other HT methods (tabbing)	2.1.1 Glass front & foil lamination (= conventional) 2.1.2 Other encapsulation concepts (including one-material & roll lamination)
	2.2 Laser soldering (tabbing)	2.2.1 Glass front & foil lamination (= conventional) 2.2.2 Other encapsulation concepts (including one-material & roll lamination)
	2.3 Conductive adhesives (large area conductive pattern or smart strips)	2.3.1 Glass front & foil lamination (= conventional) 2.3.2 Other encapsulation concepts (including one-material & roll lamination)
	2.4 Mechanical clamping (glass/low pressure/glass)	

Figure 3: Module design and assembly options considered.

4 CRYSTALCLEAR OVERALL TECHNOLOGIES

The CrystalClear overall technologies initially considered after screening are briefly described in the following (additional details are described in the (confidential) Roadmap). It is noted that technologies have recently been adjusted to include the latest insights in what is expected to be technically achievable or preferable. Since cost calculations have not yet been performed on these adjusted technologies, they are not discussed here. *The technologies presented should therefore be seen as indicative only.*

It is noted that the use of all-rear contacting schemes (in 4 of the 6 technologies) is consistent with the need for high efficiencies and considered attractive or even necessary for high-yield module manufacturing using very thin cells.

i. **Multistar**

Based on the use of cast multicrystalline silicon, feedstock cost 30 €/kg, wafer thickness 150 µm, kerf loss 140 µm, 156 x 156 mm², front & rear electrodes, encapsulated cell efficiency 17%, front-to-rear interconnects, conductive adhesives, standard lamination.

ii. **Monostar**

Based on the use of Cz monocrystalline silicon, feedstock cost 30 €/kg, wafer thickness 210 µm, kerf loss 200 µm, encapsulated cell efficiency 19%, all-rear electrodes (Interdigitated Back Contact, IBC) all-rear interconnects using “smart strips” and conductive adhesives, standard lamination.

iii. **Ribbonchamp**

Based on the use of ribbon silicon, feedstock cost 30 €/kg, wafer thickness 150 µm (no kerf loss), encapsulated cell efficiency 16%, all-rear electrodes (Metallization Wrap Through, MWT) all-rear interconnects using “smart strips” and conductive adhesives, standard lamination.

iv. **Epichamp**

Based on the use of a so-called wafer-equivalent, i.e. a thin high quality crystalline silicon layer on a low cost substrate, which may be processed like multicrystalline or ribbon silicon (with small modifications). Front & rear electrodes, cell efficiency 14%, front-to-rear interconnects using tabs and conductive adhesives, standard lamination.

v. **Superslice**

Based on the use of Cz monocrystalline silicon, feedstock cost 30 €/kg, wafer thickness 100 µm, kerf loss 140 µm, encapsulated cell efficiency 19%, all-rear electrodes (Interdigitated Back Contact, IBC) all-rear interconnects using “smart strips” and conductive adhesives, roll lamination.

vi. **(M)ultimate**

Based on the use of ribbon silicon, feedstock cost 30 €/kg, wafer thickness 100 µm (no kerf loss), encapsulated cell efficiency 18%, all-rear electrodes (Interdigitated Back Contact, IBC) all-rear interconnects using foil with patterned conductors

and conductive adhesives, glass front.

It is noted that this technology is considered to be very high risk, high potential. In other words, it will be technically extremely challenging to realize the *combined* features of this option. Nevertheless it is useful as an indicator of what might be achieved ultimately in this category of crystalline silicon cell and module manufacturing.

5 COST CALCULATIONS

The technologies outlined in the previous section have been analysed in terms of direct manufacturing costs. This has been done using typical manufacturing practice before the beginning of the project (end 2003) as a starting point and subsequently implementing modifications in materials consumption, cell processing, module assembly, cell & total area module efficiency and production scale. Yield effects have been taken into account for each process step. The effects of production scale have been estimated using the basic principles outlined in [2]. Although this report deals with thin-film photovoltaics, it contains valuable starting points for wafer-based photovoltaics as well. It is noted that we have assumed very modest economies of scale for wafer-based photovoltaics compared to thin-film photovoltaics. Our calculations may therefore give an upper limit of costs for very large scale manufacturing. In summary, when moving from small scale to very large scale production (here: from 30 MWp/yr to 1 GWp/yr) we typically use a 40-50% reduction of equipment costs, a 20-40% reduction of labour costs and a 20% reduction of materials costs.

We have assumed feedstock costs of 30 €/kg in all cases, which is considered relevant for the timeframe of the CrystalClear roadmap. Obviously lower or higher feedstock costs would have an impact on the total module manufacturing costs, but this can only be evaluated well if one considers costs in relation to quality (i.e. the cell efficiency that can be reached on the particular material). At this moment such information is not available.

In the following the results of the cost calculations are summarized. *All cost figures have been rounded to 1 digit*, consistent with the typical accuracy that can be obtained.

0. **Reference technology 2003**

A survey among a number of manufacturers has shown that direct module manufacturing costs were in the range of 2.3 to 2.6 €/Wp. This range relates to different technologies used, not to variation from manufacturer to manufacturer (which have averaged out). The typical production scale was 30 MWp/yr.

i. **Multistar**

In the absence of any scale effects, the cost is 1.7 €/Wp. Dependent on the assumptions on the economies of scale (alternatively: economies of volume) that may be achieved, the manufacturing costs are calculated to be in the range of 1.0 to 1.2 €/Wp for a production scale of 1 GWp/yr.

- ii. **Monostar**
Without scale effects the manufacturing cost is 1.8 €/Wp. Under the same assumptions on the economies of scale as used in i. the range of manufacturing costs becomes 1.1 to 1.3 €/Wp for large-scale production.
- iii. **Ribbonchamp**
See above, 1.6 €/Wp at 30 MWp/yr, 0.9 to 1.1 €/Wp at 1 GWp/yr.
- iv. **Epichamp**
This technology has not yet been analyzed.
- v. **Superslice**
See above, 1.5 €/Wp at 30 MWp/yr, 0.9 to 1.0 €/Wp at 1 GWp/yr.
- vi. **(M)ultimate**
See above, 1.6 €/Wp at 30 MWp/yr, 0.9 to 1.1 €/Wp at 1 GWp/yr.

The figures show that by the *combined effects* of technology development and economies of scale the manufacturing costs of crystalline silicon PV modules can be brought down into the range of 0.9 - 1.3 €/Wp, depending on the technology considered. It is emphasised that the lower end of this range corresponds to medium to high risk technologies. The feasibility of these technologies for large-scale production needs to be demonstrated. Particular challenges are to achieve a high overall process yield (from wafer manufacturing to module assembly) for very thin wafers, and to obtain the efficiency levels indicated in a production environment. On the other hand, the economies of scale we have assumed for very large scale manufacturing are rather modest. CrystalClear partners are therefore confident that the cost target of 1 €/Wp for modules can be reached.

6 CONCLUSIONS AND OUTLOOK

Wafer-based crystalline silicon is currently the dominant technology in the market for photovoltaics. Calculations presented in this paper show that this technology has substantial room for further reduction of module manufacturing costs, down to a level of 1 €/Wp or even less, consistent with the findings in [3]. This reduction can be achieved by a variety of cell and module approaches. Therefore we do not want to appoint a “winning” approach. It is important to note that high cell and total area module efficiencies and efficient silicon utilization are crucial to reach the cost levels indicated.

One may ask the question whether wafer-based crystalline silicon photovoltaics could reach module manufacturing costs *well below* 1 €/Wp, and possibly approach 0.5 €/Wp. The latter figure would roughly be the maximum allowable if the 2030 system price (note: not cost) targets in [1] were to be reached using this technology. The Strategic Research Agenda of the EU PV Technology Platform mentions a figure of 0.75 €/Wp for 2020, and states that a further reduction may be possible. Our calculations do not give a conclusive answer to this question, but they do give hints concerning the issues that need to, or might be addressed to move

beyond the 1 €/Wp boundary. For example, at present there seem to be no long lifetime, really low cost alternatives for regular encapsulation materials and the corresponding application methods. This also holds for all-rear contact schemes in which interconnection and encapsulation may become interlinked. This leaves us with total area module efficiency and economies of scale in module materials and processes as drivers to reduce the corresponding cost component. To reach module manufacturing costs well below 1 €/Wp it would be extremely helpful to have alternative low-cost, long lifetime module materials and processes at our disposal.

7 ACKNOWLEDGEMENTS

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8 REFERENCES

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