

SILICON SOLAR CELLS ON ULTRA-THIN SUBSTRATES FOR LARGE SCALE PRODUCTION

G. Agostinelli, P. Choulat, H.F.W. Dekkers, Y. Ma and G. Beaucarne
IMEC vzw
Kapeldreef 75, B-3001 Leuven, Belgium.

ABSTRACT: The current industrial process, based on screen printed, full coverage aluminum paste on the rear surface shows clear limitations on wafers thinner than 200 μm , due to wafer warping and decreasing cell performance. In this work we demonstrate the possibility to transfer into production an innovative process for large area silicon solar cells on 100 μm substrates. The main characteristics of this process are: an easy and straightforward way of manufacturing solar cells with a well passivated rear surface and local contacts, a great deal of integration with the existing industrial process, the compatibility with screen printed technology, the introduction of novel dry processing techniques and ultimately the potential to increase industrial solar cells efficiency on thinner substrates.

Keywords: Manufacturing and Processing, Passivation, Solar Cell Efficiencies

1 INTRODUCTION

The base knowledge in photovoltaics is that crystalline silicon is expensive and that processing thinner wafers would bring significantly lower costs and energy payback time. Yield and efficiency problems have thus far retarded the evolution towards thinner cells. It took nearly 30 years for solar cell production to move from 330-350 μm thick wafers to an average thickness of 270-280 μm in 2004, but the current silicon feedstock crisis has significantly accelerated the roadmap of wafer thinning. Wafer manufacturers provide thinner and thinner wafers as they can sell more wafers per unit mass of silicon, and cell manufacturers are eager –and obliged– to process thinner wafers as this allows them to fill their production capacity and possibly increase their margins of gain. Next year the wafers delivered to companies will have a standard thickness of 180-240 μm , and they will thin down to 150-180 μm by 2008 at the latest. Aggressive engineering may make it possible to process 150 μm wafers using full coverage Al paste, at the expenses of some percent points of efficiency [1-3]. This trend will probably progress another 2-3 years, but it is clear that this path has a limited potential for cost reduction and a limited possibility of processing thinner substrates. Going significantly thinner than 200 μm requires a technological leap to advanced solar cell structures with passivated rear surface and local contacts suitable for large scale production. The purpose of this paper is to describe how this is possible today and show pilot line results on thin (<200 μm) and ultra-thin (<150 μm) substrates.

2 THE CHALLENGE TO GO THINNER

With saturation currents in the order of $1\text{-}2\cdot 10^{-12}$ A/cm², where the emitter saturation current J_{0e} is typically $2\text{-}4\cdot 10^{-13}$ A/cm² and the base saturation current J_{0b} is easily in the pA/cm² range, industrial solar cells are base, rather than emitter, limited devices. Nevertheless most of the efforts to improve solar cell efficiencies in these years have been concentrated on the front side: texturisation, shallower emitters, reduced shadowing losses ..., the only notable exception being the adoption of SiNx:H for bulk passivation. The reason for this is that on a thick base even a large improvement of the rear

surface passivation properties would lead to a moderate increase of the cell performance. Given the absorption coefficient of silicon, the same is true for an improved rear surface reflectance on devices thicker than 250-300 μm . If we assume bulk diffusion lengths in the order of 250 μm , reducing rear surface recombination velocity from 2000 cm/s to 400 cm/s or increasing rear surface reflectance from 50% to 90% would lead to a J_{sc} increase of less than 0.8 mA/cm², combining the two things together would not add more than 1.5 mA/cm² of extra current, and 5 to 10 mV of V_{oc} . These improvements would bring and additional 0.3 to 0.6% absolute increase in efficiency, but it is questionable whether they are alone sufficient to justify the replacement of the straightforward, standard full area screen printed aluminum BSF process. Things change on thinner wafers. On a 100 μm cell, with the same parameters, we would observe a difference of more than 3 mA/cm², and 1-1.5% difference in absolute efficiency. The efficiency trade off makes the search for novel rear surface structures attractive while, at the same time, we would not be able to process these wafers with full area screen printed aluminum on a large scale because of excessive substrate bowing and consequent yield problems. This brings about the question of how to process large area solar cells on ultra-thin substrates.

The learning curve from high efficiency solar cells processing points to rear surfaces coated with dielectrics and local point contacts as the best way to achieve simultaneously a good degree of surface passivation, reflectance and a low current resistance. Realizing this in a production environment poses a few problems. The features that are used to process state-of-the-art thin cells in laboratories (thermal oxides, masking/lithography, fine line front contacts, to name a few) cannot conveniently be used in production -not on average quality material- due to problems of cost, throughput and, ultimately, possibility of integration in the standard process sequence. Other attractive solutions (SiNx:H, a-Si:H, a-SiCx:H layers, firing-through contacts) present unexpected problems when transferring the process from test structures to solar cells. R&D is still in progress, and the wafer thinning roadmap is going so fast that some cell manufacturers start to anticipate trouble. The risk is that at some point they might be offered wafers they can no longer profitably process.

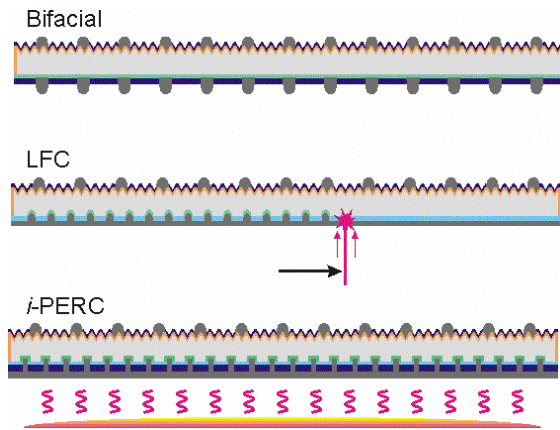


Figure 1: ongoing R&D activities on passivated rear surface solar cells on low cost substrates can be classified in three groups: bifacial solar cells with fire-through contacts, laser fired contact solar cells, and selective alloying, thermally fired LBSF solar cells (*i*-PERCs).

There are three emerging approaches that are trying to surmount this bottleneck (Figure 1): bifacial solar cells with fire-through contacts, laser fired contact (LFC) solar cells, and selective alloying, thermally fired LBSF solar cells (*i*-PERC solar cells). With the risk of disappointing the pioneers of bifacial solar cells, the first type of process has been chosen by several R&D groups for the possibility it offers of reducing the mechanical stress on the wafers and creating local contacts in a single co-firing step rather than for the clear advantages of albedo collection, which has coincidentally been re-discovered to be a plus of this type of structures. The other two approaches lead to a similar structure. They differ in that with LFC local contacts are generated by a strong heat pulse that is applied locally on a metal layer evaporated onto a passivating layer, while in *i*-PERC cells the passivation layer is structured before metallization and all the cell is subject to a rapid thermal process. In this way the local contacts are created selectively only where the metal is at contact with silicon.

i-PERC cells have already been presented in general lines at previous conferences [4,5]. In this paper we will focus on the latest results and on the technological issue of surface passivation. Essential, in *i*-PERC cells, is the presence of a thermally stable rear side passivation layer that retains its stability and surface passivation qualities during the contact firing step. Due to its characteristics this process eliminates the bowing problems when using Al screen printed paste on ultrathin wafers. Indeed, alloyed regions are formed only locally, generating small and very localized stress fields, which do not lead any significant bowing. This has been experimentally verified on large area substrates (156 cm²) as thin as 80µm.

3 SURFACE PASSIVATION

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As long as we target efficiencies of 16 to 18%, the requirements for surface passivation of solar cells on substrates down to 100µm are not as stringent as one would tend to think. Surface recombination velocities in the order of 600 to 900 cm/s with metal coverage factors up to 20% would allow for cell efficiency equal or higher to those reached on thick wafers, provided that there is an

average quality local BSF below the contacts and that the rear surface reflectance is above 80% [6]. It follows that it should be possible to work with a wide variety of dielectrics in combination with screen printed local contacts. As it has been mentioned above, things are not that easy. SiNx:H, a-Si:H, a-SiCx:H are all materials that yield very low surface recombination velocities on silicon and sometimes very high efficiency on lab cells, but have difficulties to make their way to industrial-type processes; either because in practice they fail to perform better than Al BSF, or because they cannot be integrated in the cell process (e.g. they are not thermally resistant and/or they degrade during processing). One way to go is to try to adapt the process to the passivation layers (e.g. low temperature processing for amorphous silicon, isolation of the induced floating junction for silicon nitride) but this normally brings about other issues (e.g. need for novel metallization techniques, etching/structuring steps, post-firing surface cleaning..). The other possibility is to modify the passivation layers or look for new ones.

In the past years IMEC has been extensively studying hydrogenated silicon nitride for bulk and surface passivation [7-9]. Recently, we have reported some of the major problems which arise in the integration of this material as rear surface passivation layer of solar cells [10]. The density of interface states of SiNx:H on typical solar cell surfaces (10¹¹ to 10¹² cm⁻²eV⁻¹ as measured from CV curves) is too high to ensure a good enough surface passivation in flat band or depletion conditions. This makes the work function of the electrode a problem to address. In addition, there are other recombination mechanisms in the metal/SiNx/silicon system which need to be better understood but which take part in decreasing the rear electrode performance. As a result, solar cells passivated with SiNx:H and a full area metal electrode can hardly match the efficiencies of their screen printed, full area aluminum BSF counterparts. Despite this shortcoming there are other functionalities of silicon nitride that make its use still interesting in processing thin PERC solar cells, in particular in the form of stack systems. Thin (~10nm) thermal oxides/silicon nitride stacks are known to yield very good surface passivation on silicon. This is mainly attributed to the low density of interface states of silicon, combined with the positive fixed charges due to the nitride. Yet, if they are used 'as is', in a solar cell, also these stacks don't yield as high conversion efficiency as expected. To obtain higher efficiencies, they need to be thickened, or capped by another dielectric.

We have started to study stacks of 'low quality' dielectrics and hydrogenated silicon nitride. The reason for this was the need to achieve a very good degree of surface passivation without using processes that would be harmful to the material or making the process too complicated. The intention was to exploit the hydrogen release from the SiNx:H layer during the firing step as a means of improving the surface passivation of the underlying dielectric on silicon. We found out that this is possible with various oxides and metal oxides with initial poor surface passivation qualities. Effective lifetimes of 1.5 Ohm.cm FZ wafers could be improved from a couple of microseconds to several hundreds of microseconds up to the milliseconds range after nitride deposition and firing (as measured with QSSPC at Δn=10¹⁴ cm³). With

'low quality' we mean materials that are deposited on the silicon surface -e.g. by spin coating or CVD- and/or cured at temperatures below 600° C and that, at this stage, would not be good enough to passivate the rear surface of a solar cell. These systems benefit from a field induced surface passivation which is dominated by the fixed charges present in the nitride or at the nitride/dielectric interface (in fact, in the order of 10^{11} - 10^{12} cm⁻² in nearly all stack systems). To date, we were not able to measure directly the density of interface states of the fired stacks from their GV curves due to their anomalous behaviour. From the results we obtain at device level we expect that it is significantly lower than in silicon nitrides, but this needs to be confirmed.

An additional requirement for these stacks to work at solar cell level is that they are sufficiently *thick*. It is not an optical confinement effect. And interestingly, there is no correlation between the improvements in efficiency and the surface passivation properties of the (free-to-air) stacks as measured with QSSPC in function of the stack thickness. Surface passivation is e.g. often more effective on thinner stacks. Instead the thicker the stack, i.e. the larger the displacement between the metal electrode and the silicon surface, the larger the open circuit voltage of the solar cell and its efficiency. This phenomenon has been observed consistently on different type of silicon nitride/low quality oxide stacks (Figure 2) and even nitride layers on silicon thickened by an oxide allowed for respectable V_{oc} s.

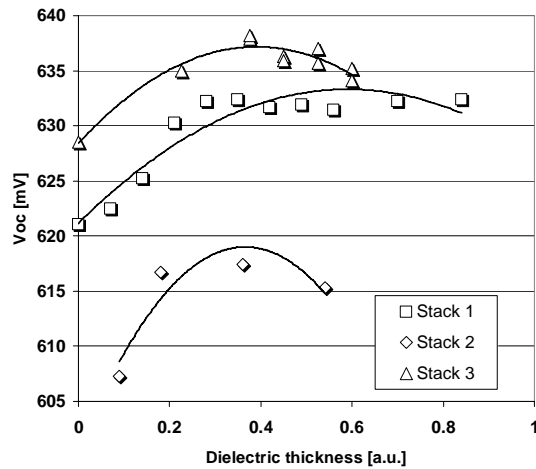


Figure 2: Open circuit voltage of iPERC cells as a function of the dielectric thickness within the dielectric/silicon nitride stack. Three different dielectric/nitride stacks are shown in the graph. The lines are a guide to the eye.

Nitride/oxide stack systems have also the remarkable characteristics of being thermally resistant. They can actually be fired several times without losing their surface passivation properties. They can also be designed in such a way that they are an effective, inert mask for metals, thereby providing a very easy way to create local BSF contacts in the underlying silicon wafer during the contact firing step. The stacks can be easily structured by laser, e.g. ablating local points with a desired pitch, and the surface damage is of no importance because it is anyway going to be alloyed. Printing or depositing aluminum over the locally ablated stack and firing provides a very simple way to create a passivated rear surface with local BSF contacts.

4 PILOT PROCESS RESULTS

One of the strengths of the *i*-PERC process is its similarity to standard screen printed cells. Indeed, the process sequence consists roughly of: surface damage removal and front side texturing by means of plasma process, POCl₃ diffusion, rear surface passivation, local point contact ablation, screen printed front and rear metallisation, contacts cofiring. With respect to a conventional line, the steps which need to be modified or introduced to process iPERC cells are:

- Single side texturing
- Dielectric deposition
- Rear surface nitride
- Laser ablation

Surface decoupling (that is, conditioning a wafer's surface so that the front is textured and the rear as flat as possible) could in principle be achieved by plasma as well as by wet chemistry. The strong point of plasma is that either by a mixed or a full plasma approach a very effective texturisation/flattening can be done by removing a very small amount of material (~2µm per side), while wet decoupling is requiring, today, more than 40-50µm of silicon. With the perspective to work on 100 µm wafers this could be a significant difference.

i-PERC solar cells are processed today in IMEC's pilot line on substrates with an average thickness of 100 to 150µm on Cz-Si and 150 to 180µm on mc-Si. Since we first presented this process average and top efficiencies are steadily improving. We can now retain not only the open circuit voltages, but also currents and therefore efficiencies down to 100µm (Figure 3). Using the pilot process, 17.3% has been reached on a large area, 105µm Cz wafer, and 16.1% on 150µm mc-Si. Top efficiencies on thin substrates are of 17.6% on 130µm thick Cz-Si and 16.6% on 180µm thick mc-Si. Absolute efficiencies are 1 up to 2% absolute higher than for reference full aluminum BSF solar cells processed in parallel.

180 µm mc-Si	Area [cm ²]	Jsc [mA/cm ²]	Voc [mV]	FF [%]	η [%]
<i>i</i> -PERC	100	33.78	623.8	78.8	16.6
Full Al BSF	100	32.7	613.9	77.6	15.6

150 µm mc-Si	Area [cm ²]	Jsc [mA/cm ²]	Voc [mV]	FF [%]	η [%]
<i>i</i> -PERC	156.25	33.57	618.7	77.4	16.1
Full Al BSF	156.25	32.36	606.6	76.9	15.1

130 µm Cz-Si	Area [cm ²]	Jsc [mA/cm ²]	Voc [mV]	FF [%]	η [%]
<i>i</i> -PERC	100	35.08	632.6	79.1	17.6
Full Al BSF	100	32.98	625.3	78.8	16.2

105 µm Cz-Si	Area [cm ²]	Jsc [mA/cm ²]	Voc [mV]	FF [%]	η [%]
<i>i</i> -PERC	100	34.84	630.4	78.7	17.3
Full Al BSF	100	31.54	624.6	76.6	15.1

Table 1: Solar cell results. All cell are tabbed, with with single layer SiNx:H ARC, 55-60 Ohm/sq emitters. Average thickness measured by weight.

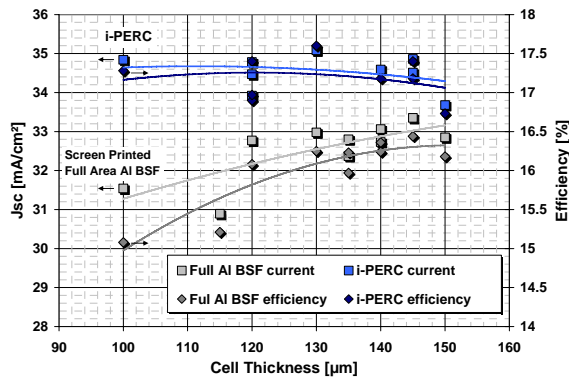


Figure 3: thinning experiment with Cz wafers. *i*-PERC solar cells maintain their efficiencies down to 100 μ m.

CONCLUSIONS

This work shows that it is possible to process silicon solar cells on ultra-thin substrates, with a technology that is suitable for large scale production. The proposed process is potentially of great importance for the PV industry. The central, short term priority for the photovoltaic market is a significant reduction of the silicon content per wafer. The silicon content is, today, roughly 13 g/Wp for mono and multicrystalline Si solar cells and around 7-8g/Wp for EFG and STR ribbons solar cells. The proposed process reduces the silicon content to figures in the order of 9g/Wp for mono and multi and would reduce it to about 3g/Wp for ribbons. First calculations indicate that this can reduce cell cost by 20% and 30%, respectively, which translates in 15% and 20% cost savings at module level. The cost reduction at system level, which ultimately determines the price per kWh of PV electricity, will be of 9-12%. Energy payback time would lower to 1.5-3 years for crystalline modules and 1-1.5 years for ribbons.

In wider terms, the ability of reducing silicon demand of 40 to 60% per watt peak has another, major spin off: it would offer the possibility for a significant market growth despite the feedstock shortage. Projections from the PV barometer of the Eurobarometer indicate that PV electricity will significantly exceed the 3GWp installation target of the Commission White Paper for 2010. The prerequisite for this to happen is that market growth continues at the pace of today. Many analysts are afraid of a significantly reduced growth in the period 2006-2010 due to the silicon shortage. Thinner wafers are a limited yet clear, quick response to compensate the lack of silicon, that can be deployed faster and in parallel to new feedstock capacity.

ACKNOWLEDGEMENTS

This work was partially funded by the European Commission under the FP6 project CRYSTAL CLEAR, contract SES6-CT-2003-502583.

This work was partially funded by Photovoltech.

The cells were measured against a reference cell which is calibrated (traceable) to the World Radiometric Reference by the European Solar Test Installation (ESTI) of the European Commission Joint Research Centre, an ISO 17025 accredited calibration laboratory

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