THE STATUS OF SILICON SOLAR CELL PRODUCTION TECHNOLOGY DEVELOPMENT AT FRAUNHOFER ISE

R. Preu, D. Biro, J. Rentsch, F. Clement, D. Erath, G. Emanuel, A. Grohe,
M. Hofmann, A. Mette, C. Voyer, W. Wolke, S.W. Glunz, G.P. Willeke
Fraunhofer Institute for Solar Energy Systems, Heidenhofstr. 2, D-79110 Freiburg, Germany
phone: +49 761 4588 5260, fax: +49 761 4588 9250, email:ralf.preu@ise.fraunhofer.de

ABSTRACT

The development of new production technologies for crystalline silicon solar cells has been very actively addressed by both research institutes and industry in the past ten years due to the increased economical value of photovoltaic energy conversion. In this paper we describe selected approaches being followed at Fraunhofer ISE in order to support the cost reduction objectives. A simple screen-printing reference process was developed with an efficiency potential of 18% for mono-crystalline silicon wafers. The set up of the Photovoltaic-Technology Evaluation Center (PV-TEC) enables a fast evaluation of new technologies on pilot scale throughput of several hundred wafers/hour.

INTRODUCTION

Since the beginning of this decade we have seen a huge progress in crystalline silicon solar cell development with significant improvements in cell efficiencies and reduction of process costs. These developments have helped to keep the learning curve of crystalline silicon solar cells on a 20% cost decrease level for doubling of the cumulated production output.

After having had a long experience in high-efficiency crystalline silicon solar cell processing and characterization at Fraunhofer ISE, the production technology group was set up in 1996. The basic idea is to start from the proof-of-concept of cell structures and processes and to realize these by means of technologies which show their potential with respect to process cost reduction. Looking at the cost of photovoltaic energy conversion a high reduction potential is mainly linked to:

- High efficiencies (mono-Si >18%, multi-Si>16%),
- high yield for thin wafers (thickness<200 µm),
- high through-put (production capacity> 50 MWp/a),
- reduced personnel and consumable cost,
- reduced environmental impact.

With respect to these boundary conditions we focus on high-efficiency cell structures, the development of processes which enable horizontal transport of wafers and therefore minimal wafer stress as well as working around the standard BSF formation with full area alloyed aluminum. For benchmarking we use standard and high-efficiency reference processes. The technology development is going through different phases, ranging from proof-of-concept to the implementation in production lines [1,2].

STANDARD PROCESS SEQUENCE

In this paper we give an overview of these developments based on technologies applied to mono-crystalline silicon wafers – almost all of them being as well applicable on multi-crystalline silicon wafers. Our standard process flow for processing Cz-Si (Czochralski-grown silicon) wafers is shown in figure 1. After a short damage etch and texturization step in an alkaline bath with organic additives, we use a tube furnace $POCl_3$-diffusion to form emitters with a sheet resistance of 40 to 55 Ω/sq. The residual phosphorus glass is removed in a short dip in hydrofluoric acid. The wafers are then deposited with a silicon nitride layer using sputter technology. Standard silver and aluminum pastes are used to define the contacts on front and rear side of the wafers, respectively. The contact is then formed in a fast firing metal-belt furnace or a rapid thermal single wafer firing furnace. Finally the wafer edge is isolated by means of laser ablation to form a shallow groove close to the wafers edge, the edge is optionally broken. With this basic process we typically reach efficiencies of up to 17.5% (undegraded) on mono-crystalline silicon wafers within a resistivity range of 0.5 to 5 Ωcm.

Function	Technology
saw damage removal / texture and cleaning	alkaline etch with organic additive
emitter formation	$POCl_3$-tube diffusion
removal of PSG and cleaning	HF etch
anti-reflection coating	sputter silicon nitride
front and rear contact deposition	screen-print of silver and aluminum layers
contact sinter	fast firing furnace
edge isolation	laser groove ablation

Figure 1: Basic functions in order to produce a solar cell and technologies used at Fraunhofer ISE for the standard process flow.

Many of the loss mechanisms of a real solar cell are interlinked in a complex way. Simple IV curve measurement techniques are in general not sufficient to separate the causes for optical, recombination, resistance and shunt losses. Specific techniques are often difficult to apply especially on a large number of wafers. For the development of new technologies it is thus very useful to use a reference process sequence which has a very high-efficiency potential. The substitution of well known process steps, e.g. the passivation quality of thermal oxides, for the evaluation of different new surface layers can be very effectively performed. Very important information can directly be deduced from the IV curve parameters as e.g. the open circuit voltage if the remaining saturation current density is sufficiently low.

The passivated emitter and rear cell with laser-fired contacts (PER-LFC) process has been developed by Glunz et al. [3,4]. Being relatively simple and robust it has demonstrated to be a very powerful tool for a high-efficiency reference cell approach. The underlying cell structure comprises a front side texturization, a shallow oxide passivated emitter, a fine and high-aspect ratio front TiPdAg contact grid and a passivated rear with LFC.

NEW TECHNOLOGIES ALREADY TRANSFERRED

Most of the reference screen-printing processes described above have already been a standard in crystalline silicon solar cell technology for years. Not so for the use of medium frequency twin magnetron sputtering of silicon nitride which we proposed as a key technology for deposition of silicon nitride in 2000 [5]. The wafers are carried on a tray through the plasma consisting of argon, sputtered silicon atoms as well as dissociation products of nitrogen and ammonia. Meanwhile we have been able to show in several round robins on pilot scale, that the sputtered anti-reflection processes perform optically and electrically on the same level as the corresponding PECVD-layers (plasma-enhanced chemical vapor deposition), both for multi- and mono-crystalline silicon. Sputtering demands more sophisticated vacuum equipment, but due to the high deposition rates the cost of ownership is very attractive for production volume levels above 50 MWp/a. It offers an improved coating uniformity on carrier and wafer and the use of the explosive gas silane is not needed [6].

A further plasma process which was used as a standard technology in silicon solar cell technology is the plasma etching of a wafer stack. This has been substituted frequently by laser ablation of a groove along the edge on the solar cells front side. We introduced the use of a double-mirror guided solid state laser beam. Due to the high beam velocity and pulse repetition rate of such laser systems we are able to isolate the complete wafer edge in approx. 1s per wafer with one laser system [7].

These two very productive processes are meanwhile transferred into equipment for solar cell production lines on a 50 MWp/a range and available from the companies Applied Films and Manz, respectively.

NEW TECHNOLOGIES DEMONSTRATED ON PILOT-SCALE

There are three basic functions which have to be fulfilled to produce a solar cell from a standard silicon wafer: formation of a separating junction, the n- and p-type electrode - approaches for technology improvements in these areas are described below.

In contrast to the standard batch type diffusion and phosphorous glass (PG) removal process we have evaluated several new tools for the in-line formation of the pn-junction. For the deposition of a phosphorus containing layer we have recently developed techniques based on ultrasonic spraying. For these deposition technologies special care was taken to select the matching material classes to be able to form uniform and clean phosphorous glass layers [8].

The diffusion process is performed in our 4-track walking string furnace featuring a very clean ambient with cleaned dry air as processing gas [9]. By substituting the $POCl_3$-diffusion of our standard process and adapting the contact firing process, we have now been able to reach efficiencies up to 17.5% on Cz silicon. These results are already in this development stage close to the level as the ones based on the $POCl_3$-diffusion.

Table 1: Parameters of solar cells processed with in-line deposition of phosphorus source and diffusion in the walking string furnace on 125×125 mm^2 Cz-Si wafers and a specific resistance of 3-6 Ωcm (texture: alkaline/IPA, plane: alkaline damage, etch only).

Surface	values	V_{oc} [mV]	J_{sc} [mA/cm²]	FF [%]	η [%]
Texture	Best	626	36.0	78	17.5
	Avg.	619	35.6	77	16.9
Plane	Best	629	33.9	79	16.9
	Avg.	628	33.8	79	16.7

Since the standard silicon nitride deposition process is typically vacuum based, it is very attractive to also perform the PG-removal process in the same system. A corresponding process has been developed recently on a pilot-scale vacuum etching tool at Fraunhofer ISE [10].

For front contact formation, we have developed a high aspect-ratio front contact technology based on the commercially available hot-melt paste [11]. The use of this type of pastes demands for several small changes in the set-up of the printer in order to keep the process conditions in the desired temperature range. Due to doubling the height and an increased conductivity of the fired contact fingers we have found a consistent improvement of 2% relative in efficiency for both mono- and multi-crystalline silicon solar cells. We have been able to achieve efficiencies of 18.0% on Cz-silicon by just replacing the standard paste in the process flow of figure 1 (see table 2).

Table 2: IV-curve parameters for solar cells printed with hotmelt paste (3-6 Ωcm p-type Cz-Si wafers, 125x125 mm²).

Values	V_{oc} [mV]	J_{sc} [mA/cm²]	FF [%]	η [%]
Best	621	36.5	79.5	18.0
Avg. of 8	620±1	36.5±0.2	78.9±0.3	17.9±0.1

A higher potential approach has been derived out of the high-efficiency technology. There the contact formation process is separated into two steps. First the contact definition and the metal/silicon contact function is achieved e.g. by fine-line, but not necessarily high aspect ratio screen-printing. Second the contact finger cross section and conductivity is increased by advanced light-induced electroplating of silver. This thickening technology is already realized successfully and currently being transferred into industry [12].

Due to the target of wafer thickness reduction and the limitations of the standard full area screen-printed aluminum alloy process, the rear contact of crystalline silicon solar cells is one of the most active R&D-fields. At Fraunhofer ISE we have been focussing on the approach of rear passivated cells with Laser Fired Contact (LFC). This approach helps to combine the high-efficiency potential of dielectric surface passivation and internal rear reflector with a high throughput contact formation process for the more than 10.000 contact points necessary per dm² wafer surface (i.e. typical processing time for one wafer is 1s). Efficiencies of up to 22% using the PER-LFC cell process has demonstrated the high potential of the LFC technology.

Currently our main research areas in this field are the development the integration of LFC in a standard screen-printed front contact firing through process as well as industrially feasible surface preparation and passivation schemes.

An efficiency exceeding 18.0% was reached for a thin mono-crystalline solar cell (thickness 170 µm, wafer format 125x125 mm²) using a thick thermal oxide and LFC [13]. Thermal oxidation passivation (wet, or thin and covered with a PECVD layer) was also successfully applied to multi-crystalline silicon wafers with an efficiency of up to 16% for a screen-printed front side. Also a new approach for wet chemical single sided surface conditioning has been used in this work [14].

A comparison of different passivation layer concepts used with the PER-LFC cell process has been given in [15]. New results in this field comprise an efficiency of 21.3% for a back side stack of amorphous silicon and silicon oxide and of 20.6% for a stack of silicon nitride and silicon oxide, all deposited by means of PECVD using the PER-LFC cell process (table 3, [16]). The LFC technology has been licensed to industrial partners in order to pursue the implementation on large scale.

Table 3: Parameters of the best high-efficiency solar cells with low-temperature dielectric passivation under one-sun illumination (0.5 Ωcm p-type Fz-Si, cell area 2x2 cm²).

Passiv. stack	V_{oc} [mV]	J_{sc} [mA/cm²]	FF [%]	η [%]
a-Si/SiO	675	39.2	80.6	21.3
SiN/SiO	670	38.8	79.8	20.6

PV-TEC: IMPROVED EVALUATION CONDITIONS

The fast-growing PV-industry asks for a fast and reliable demonstration of technological innovations on pilot-scale level. In order to support this demand we have set-up the Photovoltaic Technology Evaluation Center (PV-TEC), a new 1200 m² laboratory (Figure 2), which was inaugurated in March 2006. With PV-TEC we are able to evaluate new technologies, including all the technologies described in this paper at a hundred(s) of wafers/hour throughput. The base technology comprises the cell process sequence shown in figure 1 and can be applied to wafers of various formats including 125x125 mm², 156x156 mm² (standard) and 210x210 mm².

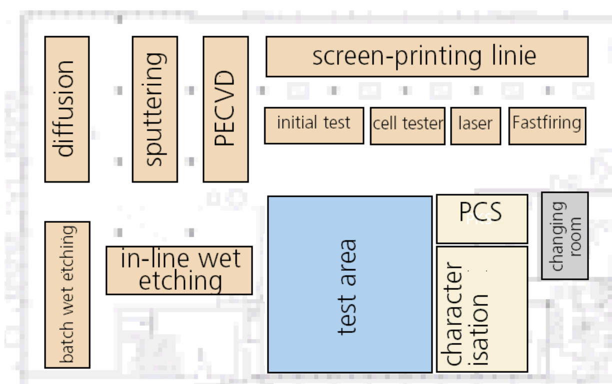

Figure 2: Schematic outline of the PV-TEC laboratory indicating the different process areas (PCS: process control system).

After a basic set-up of processes we have reached solar cell efficiencies of 15.0% for multi-Si without texturization and 16.8% for textured 0.5-2.0 Ωcm p-type Cz-Si 156x156 mm² wafers, fully processed in PV-TEC.

As described above solar cell losses are very difficult to track on a mere IV-curve analysis for a large quantity of wafers especially when cell parameters get closer to the upper limits. Furthermore, for increasing quantities of solar cells produced, a fast detection time on process problems is vital in order to receive high production yields. For these reasons in-line characterization becomes an increasingly important part of a solar cell production line. Several new approaches like in-line lifetime measurements on a wafer basis are under investigation at PV-TEC.

The full concept of the new PV-TEC facility which was set-up with strong governmental support will be described in more detail in [17].

SUMMARY AND PERSPECTIVE

ISE Several new technologies which have been developed at Fraunhofer ISE are already or currently in the stage of being transferred to industrial production of crystalline silicon solar cells, as there are:

- Sputtering of silicon nitride anti-reflection layers
- Laser-edge isolation using a scanning head
- Inline diffusion using dopants based on phosphorus acid and a walking string furnace
- Plasma etching of phosphorus glass
- Light-induced electro-plating
- Hot-melt paste front contact printing
- Laser-fired contacts

The trends in PV production technology development can be easily summarized: the objective has been and is significant cost reduction for the whole value chain. Niches for special applications will play a limited role. Thus new technologies and structures, e.g. like the upcoming back contact cells will have to be developed following the main goals: an increase of efficiency, reduction of silicon material cost and simplified module production. At least until the end of this decade there is a high number of different technologies to be investigated in order to reach the envisaged cost reduction goals. Therefore 20% efficiency for mono-crystalline silicon and 18% efficiency for multi-crystalline silicon solar cells from wafers of 150 µm thickness and a size of at least 156x156 mm² using high throughput and yield technologies should be addressed. The solar cell production technology developments approach at Fraunhofer ISE is followed to meet these goals.

ACKNOWLEDGEMENTS

The authors would like to thank for the assistance of the technicians and engineers in silicon wafer solar cell development at Fraunhofer ISE. Further, financial support by the German Federal Ministry for the Environment, Nature Conservation and Nuclear Safety (BMU) under contract No. 0329934A (SOLPRO) and 0329984 (PV-TEC) and the European Community within the Integrated Project Crystal Clear is gratefully acknowledged.

REFERENCES

[1] R. Preu, “Innovative Produktionstechnologien für kristalline Siliciumsolarzellen”, Dissertation Thesis, FernUniversität Hagen, Germany, 2000.

[2] R. Lüdemann, R. Preu, G. Willeke, "Innovation in solar cell production technology", Proc. 17th EU-PVSEC, Munich, 2001.

[3] S.W. Glunz, J. Knobloch, D. Biro, and W. Wettling, “Optimized High-efficiency solar cells with J_{SC}=42 mA/cm^2 and η=23.3%”, Proc. 14th EU-PVSEC, Barcelona, 1997.

[4] E. Schneiderlöchner, R. Preu, R. Lüdemann, and S. W. Glunz, “Laser-fired rear contacts for crystalline silicon solar cells”, Progr. Photovolt. **10** (2002) p. 29-34.

[5] R. Preu, J. Krempel-Hesse, D. Biro, D. Huljic, H. Mäckel, R. Lüdemann, “Sputtering - a key technology for thin film deposition in crystalline silicon solar cell production?”, Proc. 16th EU-PVSEC, 2000, Glasgow.

[6] W. Wolke, J. Catoir, G. Emanuel, J. Liu, M. Ruske et al., "Surface passivation for solar cells by large scale inline sputtering of silicon nitride", Proc. 20th EU-PVSEC, Barcelona, 2005.

[7] E. Schneiderlöchner, A. Grohe, S.W. Glunz, R. Preu and W. Willeke, "Scanning Nd:YAG laser system for industrially applicable processing in silicon solar cell manufacturing” , Proc. 3rd WCPEV, Osaka, 2003.

[8] C. Voyer, D. Biro, K. Wagner, J. Benick, R. Preu et al., "Progress in the use of sprayed phosphoric acid as an inexpensive dopant source for industrial solar cells", Proc. 20th EU-PVSEC, Barcelona, 2005.

[9] D. Biro, R. Preu, D. Untiedt, G. Wandel, J. Gentischer, "Transport systems for industrial in-line diffusion of silicon solar cells", Proc. 19th EU-PVSEC, Paris, 2004.

[10] J. Rentsch, C. Schetter, H. Schlemm, K. Roth, R. Preu, "Industrialisation of dry phosphorous silicate glass etching and edge isolation for crystalline silicon solar cells", Proc.20th EU-PVSEC, Barcelona, 2005.

[11] A. Mette, D. Erath, R. Ruiz, G. Emanuel, E. Kasper et al., "Hoft melk ink for the front side metallisation of silicon solar cells", Proc.20th EU-PVSEC, Barcelona, 2005.

[12] A. Mette, C. Schetter, D. Wissen, S. Lust, S.W Glunz, G.P. Willeke, “Efficiency increase of screen-printed solar cells by light-induced plating”, this conference.

[13] E. Schneiderlöchner, A. Grohe, B. Fleischhauer, M. Hofmann, S.W. Glunz, R. Preu and G.P. Willeke, "Status and advancement in transferring the laser-fired contact technology to screen-printed silicon solar cells", Proc.20th EU-PVSEC, Barcelona, 2005.

[14] J. Rentsch, O. Schultz, A. Grohe, R. Preu, "Technology route towards industrial application of rear passivated silicon solar cells", this conference.

[15] W. Glunz, A. Grohe, M. Hermle, M. Hofmann, et al.,“Comparison of different dielectric passivation layers for application in industrially feasible high-efficiency crystalline silicon solar cells”, Proc. 20th EU-PVSEC, Barcelona, 2005.

[16] M. Hofmann, S.W. Glunz, R. Preu, G.Willeke, “21%-Efficient Silicon Solar Cells Using Amorphous Silicon Rear Side Passivation”, to be published at the 21st EU-PVSEC, Dresden, 2006.

[17] D. Biro, R. Preu, S.W. Glunz et al., “PV-TEC: Photovoltaic Technology Evaluation Center - Design and implementation of a production research unit”, to be published at the 21st EU-PVSEC, Dresden, 2006.